CSE 421 Midterm Examination
Fall 2004-2005

GROUP A

Time: 60 Minutes. No extensions

Open books, open notes, closed communications. Your net score will be calculated by subtracting 1/4 of your incorrect answers from your correct answers. You may leave answers blank, except question number 14, which you must answer. All questions have the same weight.

Connecting a RAM Module

A certain 8-bit RAM module has an r-bit address bus. It is connected to a microprocessor that has an a-bit address bus. The number of direct address line connections is c (lines 0 through $c-1$). (That is, c address lines are connected directly with each other.) There are d adress lines on the microprocessor side that are **properly** decoded and connected to the chip select inputs of the RAM module.

1. The size of the RAM module is:

(a) 2^a bytes **(b)** 2^{a-r} bytes **(c)** 2^r bytes **(d)** 2^{r-1} bytes **(e)** 2^{a-d} bytes

2. The fraction of total bytes in the RAM module that can be addressed by the microprocessor is:

(a) 2^{-c} **(b)** 2^{r-a} **(c)** 2^{d-a} **(d)** 2^{r+d-a} **(e)** 2^{c-r}

3. The number of mirror images of this RAM module is:

(a) 2^{a-r+d} **(b)** 2^{a-c-d} **(c)** 2^{a-d} **(d)** 2^{a-c+d} **(e)** 2^{a-r-d}

4. On the microprocessor's memory map, how many bytes map to this RAM module?

(a) 2^{a-d} bytes **(b)** 2^c bytes **(c)** 2^r bytes **(d)** 2^{r-d} bytes **(e)** 2^{a-c-d} bytes

About the PIA...

A PIA is connected to a 6800-series microprocessor and is mapped to locations $2000 – $2003.

The following instructions are executed:

```
LDAA $2001
LDAB $2000
```

At the end of the two instructions, accumulator A contains $\$A6$ and accumulator B contains $\$00$.

5. According to the information given above, which of the following statements are true?

I. Control line CA1 is set up to detect a positive transition.

II. Control line CA2 is in pulse mode.

III. Port A of the PIA is definitely set up to be all inputs.

(a) Only I **(b)** Only II **(c)** Only III **(d)** I and III **(e)** I, II, and III

6. Given that the IRQA line of the PIA is connected to the IRQ input of the microprocessor, which of the following statements are true?

I. A transition has been detected on CA1

II. An IRQ interrupt has been generated by the PIA

III. If a `LDAA $2001` instruction is executed *again* after the two given instructions, we will *definitely* get the value $\$A6$ again.

(a) Only I **(b)** Only II **(c)** I and II **(d)** II and III **(e)** I, II, and III

7. After the two given instructions are executed, CA2 will...

(a) ... be unaffected.
(b) ... will go low for a short time.
(c) ... will go high for a short time.
(d) ... will go low until the next transition detection on CA1.
(e) ... will go high until the next transition detection on CA1.

About the ACIA

An ACIA is known to operate with a 19200.0 Hz clock. At power-on, the following code is executed:

```
LDAA #$43
STAA $3000
LDAA #$9A
STAA $3000
```

8. How long does it take to transmit one byte?

(a) 3/100 sec. **(b)** 1/240 sec. **(c)** 3/400 sec. **(d)** 2/75 sec. **(e)** 1/30 sec.

9. Which of the following values may the status register NOT have?

(a) $\$0C$ **(b)** $\$CC$ **(c)** $\$8E$ **(d)** $\$8F$ **(e)** $\$AD$

10. On which of the following conditions will the ACIA generate an interrupt?
I. Receive data register is full.
II. Transmit data register is empty.
III. A framing error has occured.

(a) I and II **(b)** II and III **(c)** I and III **(d)** None **(e)** I, II, and III

Miscellaneous

11. The analysis of a certain 6800-series system reveals that, it may call at most five nested subroutines and may need to service two levels of nested interrupts. Every subroutine saves the registers A, B, and X on the stack when called, and restores them from the stack before returning. How much of stack space is needed just for these needs?

(a) 24 **(b)** 30 **(c)** 38 **(d)** 44 **(e)** 50

12. For a certain application, you need an A/D converter. Your input to the converter will be in the range of 0 to 9 volts, and you wish to be able to detect a voltage change of 0.01. Which of the following A/D converters would you choose? (Assume ranges start at 0V and go up where not given.)

(a) 8 bits, 0-9V range **(b)** 10 bits, 0.005V precision
(c) 11 bits, 0-20V range **(d)** 12 bits, 0.2V precision **(e)** 12 bits, 0-5V range

13. For which of the following reasons should one use a hardware timing circuit instead of a software timing loop?
I. The system has to process many interrupts.
II. The system performs a job that requires high processing power.
III. The clock speed is very high.

(a) Only I **(b)** Only III **(c)** I and III **(d)** I and II **(e)** I, II, and III

14. Which of the following statements are true?
I. I did not cheat on this exam.
II. I did not let anyone cheat in this exam.
III. I did not see anyone cheat in this exam.

(a) None **(b)** Only I **(c)** I and II
(d) I, II, and III **(e)** I, II, and III and the exam was too hard.